REMARKS

Claims 86-101 are now pending in the application. While Applicants disagree with the current rejections, Applicants have amended the claims to expedite prosecution. Applicants reserve the right to pursue the claims as originally filed in one or more continuing applications. Claims 1-85 are cancelled. Claims 86-101 are new. Support for the new claims can be found throughout the drawings and specification as originally filed. Therefore, no new matter has been added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 112

Claims 1-6 and 48-62 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter that Applicants regard as the invention. This rejection is respectfully traversed.

Claims 1-6 and 48-62 are cancelled. Accordingly, the rejections of these claims are rendered moot.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-6, 48-50, 52-57, 59-61, and 63-85 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,662,253 ("Gary") in view of U.S. Pub. No. 2002/0184453

("Hughes"). Claims 7, 51, 58, and 62 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gary in view of Hughes, as applied to claims 6 and 57 above, in further view of U.S. Pat. No. 6,745,274 ("Snyder"). These rejections are respectfully traversed.

Claims 1-7 and 48-85 are cancelled. Accordingly, the rejections of these claims are rendered moot.

NEW CLAIMS

Claim 86 recites, inter alia, a speed matching FIFO memory module configured to i) receive first data from the first processor over the first bus via the first interface in the first frequency domain, and ii) receive second data from the second processor over the second bus via the second interface in the second frequency domain.

None of the cited prior art references appear to disclose a speed matching FIFO memory module as recited in claim 86. For example, the Examiner relies on FIG. 3 of Gary to disclose a peripheral I/O register 301, which purportedly corresponds to a speed matching module. (See Page 5 of the Office Action mailed May 21, 2010, hereinafter "the Office Action").

Initially, Applicants respectfully submit that the peripheral I/O register 301 is not a FIFO memory module as claim 86 recites, which the Examiner acknowledges. (See Page 6 of the

Office Action). Further, the peripheral I/O register 301 does not receive first data from the first processor over the first bus via the first interface in the first frequency domain, and receive second data from the second processor over the second bus via the second interface in the second frequency domain.

Further, Hughes fails to make up for the deficiencies of Gary. For example, the Examiner relies on Paragraph [0003] of Hughes to disclose that different cores "communicate with each other only by way of the shared memory." Applicants respectfully submit that Hughes is absent of any teaching or suggestion that the shared memory is a FIFO memory module that receives first data from the first processor over the first bus via the first interface in the first frequency domain, and receives second data from the second processor over the second bus via the second interface in the second frequency domain.

Applicants respectfully submit that claim 86 is allowable for at least these reasons. Claim 94 includes similar subject matter and is allowable for at least similar reasons. Claims 87-92 and 95-101 depend from claims 86 and 94 and are allowable for at least similar reasons.

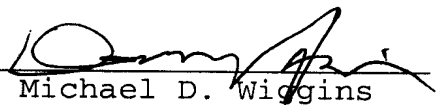
CONCLUSION

It is believed that all of the stated grounds of rejection have been properly addressed. For all of the reasons set forth above, Applicants submit that the application is in condition for allowance. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. By addressing particular positions taken by the Examiner in the above remarks, Applicants do not acquiesce to other positions that have not been explicitly addressed. In addition, Applicants' arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

If the Examiner believes that personal communication will allow any outstanding issues to be resolved, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: August 20, 2010

By: 

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